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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,426	01/16/2008	**Harald Jacobsson**	0110-091	9268

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EXAMINER	
PATEL, DHAVAL V	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
06/23/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/595,426	JACOBSSON ET AL.	
	Examiner	Art Unit	
	DHAVAL PATEL	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 48-53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 48 recites the limitation "the step of resetting the analog VCO control voltage" in line 1. There is insufficient antecedent basis for this limitation in the claim, in claim 47, step d, it recites about settles the analog VCO within the narrower window, however, does not recites "step of resetting" .

Claim 49 recites the limitation "the step of adjusting the analog VCO control voltage" in line 1. There is insufficient antecedent basis for this limitation in the claim. In claim 47, step d, it recites about settles the analog VCO within the narrower window, however, does not recites “step of adjusting".

Claims 51-53 are rejected because of dependent upon claim 49 and claim 49 is rejected.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: ***(See MPEP Ch. 2141)***

a. Determining the scope and contents of the prior art;
b. Ascertaining the differences between the prior art and the claims in issue;
c. Resolving the level of ordinary skill in the pertinent art; and
d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

4. **Claims 28-31, 34, 42, 43, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lam et al. (US 6,806,786) (hereafter Lam) in view of Kaufmann et al. (US 2003/0050029) (hereafter Kaufmann)**

Regarding claims 28 and 47, Lam discloses a multi-band Phase-Locked Loop (PLL) arrangement (Fig. 1, multi band VCO) and method, comprising: a single-loop PLL including a phase/frequency detector (Fig. 1, phase frequency detector, 120), a loop filter (Fig. 1, 130), a Voltage- Controlled Oscillator (VCO) (Fig. 1, VCO, 140), and a reference voltage signal (Vref) input to the arrangement (Fig. 1, reference signal source, 110);

a control circuit (Fig. 1, control unit, 150) for locking the VCO to a correct frequency band (Fig. 1, control unit 150 sends band_sel signal to VCO to lock), the control circuit (Fig. 1, control unit, 150) including a multi-window circuit (Fig. 1, 150a) having at least two amplitude windows, each amplitude window being defined by respective upper and lower voltage levels (col. 7 lines 53-55, the high and low

threshold values respectively define the upper and lower limits of the control voltage); and

a comparison device (Fig. 4, comparators, 410a and 410b) for comparing a VCO control voltage output (Fig. 4, Vcomp) from the loop filter (Fig. 1, 130) with the upper and lower voltage levels of an amplitude window (Fig. 4, comparators 410a and 410b compares the Vcomp from loop filter with the Vhigh and VLow (higher and lower voltage levels which is also considers an amplitude window);

if the VCO control voltage does not settle within an amplitude window, the comparison device provides a signal for providing a second control signal to the VCO for switching the VCO to another frequency band; and for the other frequency band, the VCO control voltage signal is compared with at least one of the amplitude windows to determine if phase lock is achieved in the other frequency band (Fig. 1 and 4, col. 7 lines 1-7 discloses if the PLL is operation then it would attempt to lock the frequency/phase of the VCO to that of reference signal. in particular PLL adjusts the control voltage signal to move the frequency of the VCO towards the frequency of the reference signal. for a multi-band VCO, each frequency band covers a particular range of frequencies for the control voltage signal col. 7 lines 9-15 discloses if the frequency of the reference signal is within range of the selected frequency band, then the control voltage signal will be adjusted by the PLL within the range defined by maximum and minimum limits, if the frequency is outside the range, control voltage is adjusted outside the range. the control voltage will be moved either upper or lower rail by the PLL).

However, Lam does not explicitly disclose wherein if the VCO control voltage settles within a first amplitude window, a second narrower amplitude window is selected and the VCO control voltage is compared with the upper and lower voltage levels of the second amplitude window; if the VCO control voltage settles within the second amplitude window or a further subsequent even narrower amplitude window, phase lock is achieved;

In the same field of endeavor, Kaufmann teaches fast locking wide band frequency synthesizer in which frequency synthesizer incorporates a VCO having band switching capability, page 1, [0014] teaches synthesizer utilizes a VCO having a plurality of bands whereby each band comprises a narrow range of frequency within a limited tuning range. each band covers a small potion of frequency range and page 5, [0061] teaches if optimum band is not selected , the controller choose another band (interpretation:-here, all frequency bands has difference frequency range so, if one frequency range is not selected , the next frequency range could be of small range (smaller window operation) to achieve the frequency lock), because each band works in maximum and minimum frequency, it could be different frequency range, therefore, different window operation, and page 5, [0068] teaches next band is either lower or higher band.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to combine the teachings of Kaufmann, into the system of Lam, as a whole, so as to tuning the VCO voltage within the higher or lower frequency band (higher or lower window operation) based on if VCO tunes within the frequency range of

current frequency range or not and switching to the another band if not tunes within current window, the motivation is to provide frequency synthesizer with fast locking and permits use of band switching VCO for its frequency control output (page 1, [0001]).

Regarding claim 29, Lam further discloses the arrangement, wherein the VCO control voltage comprises an analog signal (Fig. 1, Vcomp, and control voltage signal).

Regarding claim 30, Lam further discloses the arrangement, wherein the second control signal comprises a digital signal (Fig. 1, band_sel, col. 9 lines 13-14)

Regarding claim 31, Lam further discloses the arrangement, wherein the comparison device (Fig. 4, 150a) comprises first and second comparators (Fig. 4, 410a and 410b) for comparing the VCO control voltage with the upper voltage level and the lower voltage level, respectively (Fig. 4, comparator generates high and low signal after comparing the control voltage with high and low limits),

But, Lam does not explicitly disclose if the VCO control voltage exceeds the upper voltage level or is below the lower voltage level, a corresponding signal is provided to a switching enabler to indicate whether a switch is to be done to a higher frequency band or to a lower frequency band.

In the same field of endeavor, Kaufmann teaches comparing the tuning voltage with the reference voltage (Fig. 11, step 130) and configure VCO with the next higher band that covers the desired channel and configure VCO with the lower band that

covers the desired channel based on whether the tuning voltage is below reference voltage or not.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to combine the teachings of Kaufmann, into the system of Lam, as a whole, so as to switching the VCO to the higher or lower band based on comparing the VCO control voltage with the reference voltage (as maximum and minimum limits), the motivation is to the motivation is to provide frequency synthesizer with fast locking and permits use of band switching VCO for its frequency control output (page 1, [0001]).

Regarding claim 34, Lam further discloses the arrangement of claim 28, wherein when phase lock has been achieved, amplitude window having an arbitrary size can be selected from the amplitude windows available in the multi-window circuit (col. 5 lines 54-65, various ranges and center of each frequency in overlap frequency bands).

Regarding claim 42, Lam further discloses the arrangement of claim 28, wherein the single-loop PLL is a narrowband PLL (Fig. 1).

Regarding claim 43, Kauffman further discloses the arrangement of claim 34, wherein upon achieving phase lock, an amplitude window larger than a smallest amplitude window within which phase lock was achieved is selected as an operation window (Fig. 11, page 4, [0046] , [0052] and page 6, [0072]).

Regarding claim 48, further comprising the step of resetting the analog VCO control voltage when there is a switch of frequency band (col. 2 lines 48-56).

5. **Claims 32-33, 35-37 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lam and Kaufmann, as applied to claim 28 and 47 above, and further in view of Su et al. (US 2002/00893873) (hereafter Su).**

Regarding claims 32 and 50, the combined teachings of both Lam and Kaufmann do not explicitly disclose the arrangement of claim 31, wherein the comparison device is connected to a first delay device such that if a switch is to be done to another frequency band, the corresponding signal is clocked into the switching enabler after lapse of a time period.

In the same field of endeavor, Su teaches synthesizer with lock detector, locking extended range VCO. page 4, [0052] teaches if after a lock condition exists, that lock conditions then lost, the range of control voltages for the curve that was being used at the time the lock condition was lost is checked to determined if lock condition can be reestablished and if not then switching to the next curve or next frequency range, here, the examiner has construed as if the control voltage is not within the range of the window that it compares to, the process is over and it switches to the next frequency band to see if control voltage is within that range is or not.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention combine the teachings of Su, into the system of both Lam and Kaufmann, as a whole, so as to switching after lapse of time if lock condition does not

exists to another frequency range, the motivation is to systematically obtain a lock condition after lock condition has been lost or existed (page 1, [0012]).

Regarding claim 33, the combined teachings of Lam and Kauffman do not explicitly disclose the arrangement of claim 32, wherein the switching enabler comprises a state machine that provides the second control signal to the VCO based on the clocked signal from the switching enabler.

In the same field of endeavor, Su teaches page 4, [0052] , that switching from one band to another band after lock condition is lost and also teaches the state machine has performed such functions is performed by the controller which has state machine to tune the VCO to the lower or higher curve or frequency ranges.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to combine the teachings of Su, into the system of both Lam and Kauffman, as a whole, so as to band switching of VCO using state machine, the motivation is to systematically obtain a lock condition after lock condition has been lost or existed after period time (page 1, [0012]).

Regarding claim 35, the combined teachings of Lam and Kaufmann do not explicitly disclose the arrangement of claim 28, wherein the control circuit comprises a lock detection circuit for continuously monitoring whether phase lock has been achieved.

In the same field of endeavor, Su teaches synthesizer with lock detector, locking extended range VCO. page 4, [0052] teaches if after a lock condition exists, that lock conditions then lost, the range of control voltages for the curve that was being used at the time the lock condition was lost is checked to determined if lock condition can be reestablished and if not then switching to the next curve or next frequency range.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention combine the teachings of Su, into the system of both Lam and Kaufmann, as a whole, so as to switching after lapse of time if lock condition does not exists to another frequency range, the motivation is to systematically obtain a lock condition after lock condition has been lost or existed (page 1, [0012]).

Regarding claim 36, the combined teachings of Lam and Kauffman do not explicitly disclose the arrangement of claim 35, wherein the lock detection circuit comprises an initialize that restarts the control circuit with the first amplitude window if phase locking is not achieved or if phase lock is lost.

In the same field of endeavor, Su teaches lock detection and algorithm in which in page 4, [0052] that if after a lock condition exist, the lock condition is lost, , the range of control voltages for the curve that was being used at the time the lock condition was lost is checked to determined whether a lock condition is reestablished by a state machine (restarts the operation).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to combine the teachings of Su, into the system of Lam and

Kaufmman, as a whole, so as to initialize the operation or reestablish the operation when the lock condition is lost , the motivation is to systematically obtain a lock condition after a lock condition is lost (page 1, [0012]).

Regarding claim 37, the combined teachings of Lam, Kaufmann and Su teaches the arrangement, wherein the lock detection circuit uses signals output from the comparison device and from the multi-window circuit (Lam, Fig. 4, multi window circuit, comparing the control voltage with upper and lower voltage of amplitude window) to establish if the VCO control voltage falls within an amplitude window, such that if the VCO control voltage does not fall within the amplitude window, the initialize restarts the control circuit, otherwise a lock-achieved condition is indicated (Lam, col. 7 lines 9-21 teaches if the VCO control voltage is outside the range than control signal would be adjusted by moving to either the upper or lower rail by the PLL as it attempts to adjust the frequency of the VCO and Su teaches page 4, [0052] if the lock condition does not exists, restart or reestablish the connection with the same curve (frequency range) and if not, switch to the another band).

6. **Claims 38-41 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lam et al and Kaufmann, as applied to claims 31 and 47 above, and further in view of Gupta et al. (US 6,778,024) (hereafter Gupta).**

Regarding claims 38 and 49, the combined teachings of both Lam and Kauffman do not explicitly disclose the arrangement of claim 31, further comprising a loop switch

arrangement having a threshold circuit for adjusting the VCO control voltage to substantially assume a desired voltage within an amplitude window after frequency band switching.

In the same field of endeavor, Gupta teaches when the tune signal exceeds one of the threshold voltages, the circuit increments or decrements the signal, this in turn changes the voltage-to-frequency characteristics of the VCO so that another curve K is selected, further the trim signal is conditioned such that PLL will maintain the lock on the frequency during the change of the characteristics and in one embodiments, the VCO drifts from a current operating curve to a new operating curve such that the PLL remains locked during the transition (col. 4 lines 14-25).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to combine the teachings of Gupta, into the system of Lam and Kauffman, as a whole, so as to adjust the threshold voltage when VCO drifts from a current curve to a next operating curve to keep the PLL locked during transition, the motivation is to keep the PLL in locked state during the adjustment of VCO (col. 2 lines 20-23).

Regarding claims 39 and 40, the combined teachings of Lam, Kauffman and Gupta do not explicitly disclose the arrangement of claim 38, wherein the threshold circuit controls a switching arrangement comprising two transistors for charging or discharging a VCO control voltage control point, depending on whether adjustment of the VCO control voltage upwards or downwards is needed, using a supply voltage or

ground until the VCO control voltage substantially assumes a desired voltage within the amplitude window, however, one of ordinary skilled in the art would easily recognized that by charging or discharging the transistors , one can adjust the VCO control voltage upwards or downwards or by adjusting the charging the transistors more to adjust the VCO voltage upward and discharging the other transistors downwards to reduce the voltage towards downwards or grounding the voltage to reduce the voltage of VCO control signal, therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to move control point upwards or downward by charging or discharging the transistors the motivation is to control the VCO voltage within certain range, as well known in the art.

Regarding claim 41, Lam further discloses the arrangement, wherein a single supply voltage is a used (Fig. 1 and 2).

7. **Claims 44, 45 ,51-53 are is rejected under 35 U.S.C. 103(a) as being unpatentable over Lam, Kaufmann and Gupta, as applied to claims 39 and 49 above, and further in view of Creed et al. (US 6,664,826) (hereafter Creed).**

Regarding claims 44, 45, 51-53, the combined teachings of Lam, Kauffman and Gupta do not explicitly disclose the arrangement of claim 39, wherein the control point is located in the loop filter and wherein the loop filter is an active filter that includes an amplifier and the control point is located before the amplifier.

In the same field of endeavor, Creed teaches loop filter and amplifier for improved phase margin and decrease phase noise, in which it teaches loop filter and amplifier is configured to generate a control voltage (control point) by shifting the control voltage by an amount determined by offset voltage and by adjusting the control voltage of a correction voltage, here, the control point is construed as before amplifier (Fig. 3, loop filter and amplifier, 206), here, the loop filter is construed as active filter

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to combine the teachings of Creed, into the system of Lam, Kauffman and Gupta as a whole, so as to loop filter and amplifier to tune or control the VCO range, the motivation is to maintain the stability of the loop (col. 2 lines 10-14).

8. **Claims 46 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lam and Kaufmann, as applied to claims 28 and 47 above, and further in view of Turner et al. (US 6,396,890) (hereafter Turner).**

Regarding claims 46 and 54, the combined teachings of Lam and Kauffman do not explicitly disclose the arrangement of claim 28, wherein the single-loop PLL includes a charge-pump PLL that includes a charge storage device, the VCO control voltage is based on charging and discharging of the charge storage device, and the loop filter is a passive filter.

In the same field of endeavor, Turner teaches that the charge pump is disabled and the loop filters resistors are shorted to create the signal capacitor, the passive loop

filter 4 is connected via one of two switches to either a voltage Vco or to a ground in order to change or discharge the loop filter as appropriate

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to combine the teaching of Turner, into the system of both Lam and Kauffman, as a whole, so as to having frequency synthesizers with passive loop filter to charge or discharge storage elements (capacitance), the motivation is to improve the functionality of the synthesizer (col. 6 lines 57-59).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patel Dhaval whose telephone number is (571) 270-1818. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. Customer Service can be reached at (571) 272-2600. The fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Dhaval Patel/

Examiner, Art Unit 2611

6/9/2009

/Shuwang Liu/

Supervisory Patent Examiner, Art Unit 2611